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Claims

[c1] 1. A low-temperature polysilicon thin film transistor (LTPS-TFT), adapted to be disposed on a substrate, the LTPS-TFT comprising:

a gate disposed on the substrate;

a gate dielectric layer disposed on the substrate and the gate;

a patterned silicon layer disposed on the gate dielectric layer and over the gate, wherein the patterned silicon layer comprises a polysilicon channel region and an amorphous silicon hot carrier restrain region adjacent thereto;

a patterned insulating layer disposed on the patterned silicon layer;

an ohmic contact layer disposed on a portion of the patterned silicon layer other than the polysilicon channel region and the amorphous silicon hot carrier restrain region and a portion of the insulating layer over the amorphous silicon hot carrier restrain region to expose a portion of the patterned insulating layer; and

a source/drain layer disposed on the ohmic contact layer.

[c2] 2. The LTPS-TFT of claim 1, further comprising a passivation layer disposed on the source/drain layer to cover the patterned insulating layer.

[c3] 3. The LTPS-TFT of claim 1, wherein the ohmic contact layer comprises an n-type ohmic contact layer or a p-type ohmic contact layer.

[c4] 4. The LTPS-TFT of claim 1, wherein the material of the insulating layer comprises silicon oxide or silicon nitride.

[c5] 5. A method of fabricating a LTPS-TFT, comprising:
forming a gate on a substrate;
forming a gate dielectric layer on the substrate and the gate;
forming a first amorphous silicon layer, a patterned insulating layer and a second amorphous layer over the gate sequentially, wherein the patterned insulating layer is formed on a portion of the first amorphous silicon layer and over the gate, and the second amorphous silicon layer is formed on the first amorphous and the patterned insulating layer;
patterning the first amorphous silicon layer and the second amorphous silicon layer to form a first patterned amorphous layer and a second patterned amorphous layer to expose a portion of the gate dielectric layer, wherein the second patterned amorphous silicon layer

exposes a portion of the patterned insulating layer;
melting and then recrystalizing a portion of the first patterned amorphous silicon layer to form a polysilicon channel region over the gate, wherein the first patterned amorphous silicon layer under an overlap of the second patterned amorphous and the patterned insulating layer becomes an amorphous silicon hot carrier restrain region; and
forming a source/drain layer on the second patterned amorphous silicon layer.

[c6] 6. The method of fabricating a LTPS-TFT of claim 5, wherein the step of forming the polysilicon channel region further comprises performing a laser annealing process.

[c7] 7. The method of fabricating a LTPS-TFT of claim 6, wherein the laser annealing process comprises an excimer laser annealing process.

[c8] 8. The method of fabricating a LTPS-TFT of claim 5, wherein further comprising doping a portion of the first amorphous silicon layer after forming the patterned insulating layer and before forming the second amorphous silicon layer.

[c9] 9. The method of fabricating a LTPS-TFT of claim 5,

wherein further comprising doping another portion of the first amorphous silicon layer and the second amorphous silicon layer after forming the second amorphous silicon layer and before forming the source/drain layer.

[c10] 10. The method of fabricating a LTPS-TFT of claim 9, wherein further comprising doping the another portion of the first patterned amorphous silicon layer and the second patterned amorphous silicon layer after forming the polysilicon channel region and before forming the source/drain layer.

[c11] 11. The method of fabricating a LTPS-TFT of claim 10, wherein further comprising performing an annealing activation process for the another portion of the first amorphous silicon layer and the second patterned amorphous silicon layer after doing the another portion of the first amorphous silicon layer and the second patterned amorphous silicon layer and before forming the source/drain layer.

[c12] 12. The method of fabricating a LTPS-TFT of claim 5, further comprising forming a passivation layer over the source/drain layer to cover the insulating layer.

[c13] 13. The method of fabricating a LTPS-TFT of claim 5, further comprising melting and then recrystalizing the

second patterned amorphous silicon layer while forming the polysilicon channel region.

[c14] 14. A The method of fabricating a LTPS-TFT , comprising:

forming a gate on substrate;

forming a gate dielectric layer on the substrate and the gate;

forming a first amorphous silicon layer, a patterned insulating layer and a second amorphous layer over the gate sequentially, wherein the patterned insulating layer is formed on a portion of the first amorphous silicon layer and over the gate, and the second amorphous silicon layer is formed on the first amorphous and the patterned insulating layer;

patterning the first amorphous silicon layer and the second amorphous silicon layer to form a first patterned amorphous layer and a second patterned amorphous layer to expose a portion of the gate dielectric layer, wherein the second patterned amorphous silicon layer exposes a portion of the patterned insulating layer;

forming a source/drain layer on the second patterned amorphous silicon layer; and

melting and then recrystalizing a portion of the first patterned amorphous silicon layer to form a polysilicon channel region over the gate, wherein the first patterned

amorphous silicon layer under an overlap of the second patterned amorphous and the patterned insulating layer becomes an amorphous silicon hot carrier restrain region.

[c15] 15. The method of fabricating a LTPS-TFT of claim 14, wherein the step of forming the polysilicon channel region further comprises performing a laser annealing process.

[c16] 16. The method of fabricating a LTPS-TFT of claim 15, wherein the laser annealing process comprises an excimer laser annealing process.

[c17] 17. The method of fabricating a LTPS-TFT of claim 14, wherein further comprising doping another portion of the first amorphous silicon layer after forming the patterned insulating layer and before forming the second amorphous silicon layer.

[c18] 18. The method of fabricating a LTPS-TFT of claim 14, wherein further comprising doping another portion of the first amorphous silicon layer and the second amorphous silicon layer after forming the second amorphous silicon layer and before forming the source/drain layer.

[c19] 19. The method of fabricating a LTPS-TFT of claim 18, further comprising performing an annealing activation

process for the another portion of the first amorphous silicon layer and the second patterned amorphous silicon layer after doing the another portion of the first amorphous silicon layer and the second patterned amorphous silicon.